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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,979	12/31/2001	Toshio Miyamoto		6075

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,979	MIYAMOTO ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/499,618.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/3/04 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 49-74 have been considered but are moot in view of the new ground(s) of rejection.

In regards to " soldering simultaneously the first semiconductor devices and the second semiconductor device on the module board ". One skilled in the art would readily recognize to simultaneously soldering the first semiconductor devices and the second semiconductor device to mount them on the module board after the step of arranging the first semiconductor devices and the second semiconductor device on the module board after the step of arranging the first and second devices of Carpenter, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module.

In regards to Carpenter teaching semiconductor devices 58 having protruded terminals as external terminals. Carpenter clearly teaches semiconductor devices 58

having protruded terminals (i.e. solder attachments) as external terminals (see col. 4 lines 9-15).

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the **wherein a minimum pitch of the bonding electrodes is larger than a minimum pitch of the protruded terminals of respective first semiconductor device** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 61 and 73 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 61 and 73 both recite **a minimum pitch of the bonding electrodes is larger than a minimum pitch of the protruded terminals of the respective first device**. The specification on pages 15-17, 31,62, 63, and 65 states that the pitch of the bonding electrodes is smaller than a minimum pitch of the protruded terminals of the respective first device.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 49-62 and 73 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. In claim 49, the phrase " protruded terminals suits the wiring rule on a module board " is vague and indefinite since it is not clear from the claim what is meant by wiring rule.

9. In claim 61, the phrase " a minimum pitch of the bonding electrodes is larger than a minimum pitch of the protruded terminals of the respective first device " is vague and indefinite since it is not clear how the above phrase is possible since claim 49 recites that the pitch of the protruded terminals is wider than the pitch of the bonding electrodes of the DRAM semiconductor chip.

10. In claim 73, the phrase " a minimum pitch of the bonding electrodes is larger than a minimum pitch of the protruded terminals of the respective first device " is vague and indefinite since it is not clear how the above phrase is possible since the specification on page 15 states that the pitch of the bonding electrodes is smaller than a minimum pitch of the protruded terminals of the respective first device.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 49-60, 62-72, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter (U.S. 5,541,448) in view of Mori (U.S. 5,604,379).

With the respect Claims 49, 57, 58, 59, 63, and 71, Carpenter discloses providing a plurality of first semiconductor devices 58 each having a DRAM semiconductor chip and protruded terminals as external terminals. A second semiconductor device has a package body, a nonvolatile memory semiconductor chip (i.e. EPPROM) sealed in the package body and outer leads protruding outwardly from a side surface of the package body. As stated in col. 1 lines 16-24 and col. 4 lines 16-23, any one of the electronic devices can be EPROMs or DRAMs. Mounting the first semiconductor devices 58 and the second semiconductor device 60 on the module board, wherein the mounting step is performed such that the protruded terminals of the first semiconductor devices 58 are arranged at the inside of the DRAM semiconductor chips of the first semiconductor devices in a plan view. Each of the protruding terminals is soldered to terminals of the board 52 (see col. 4 lines 3-23; Figs. 5 and 6). Carpenter fails to explicitly disclose a rewiring layer for electrically connecting the protruded terminals to bonding electrodes of the first semiconductor chip and setting the pitch of the protruded terminals to be wider than the pitch of the bonding electrodes of the chip so that the pitch of the protruded

terminals suits the wiring rule (i.e. pattern) on a module board. However, Mori discloses a rewiring layer 4, 5 for electrically connecting the protruded terminals 8 to bonding electrodes 2 of the first semiconductor chip 1a and setting the pitch of the protruded terminals to be wider than the pitch of the bonding electrodes of the chip so that the pitch of the protruded terminals suits the wiring rule (i.e. pattern) on a module board 18 (see col. 4 lines 47-67 and col. 6 lines 1-43; Figs. 3-11). Thus, Carpenter and Mori have substantially the same environment of chip attached to a substrate by solder connection. Therefore, one skilled in the art at the time of the invention would readily recognize substitute the chip with protruding terminal wider than the pitch of the electrodes for the first chip of Carpenter, since the chip with protruding terminal wider than the pitch of the electrodes would prevent short circuiting between adjacent protruding terminals while reducing the size of the chip as taught by Mori. One skilled in the art would readily recognize to simultaneously soldering the first semiconductor devices and the second semiconductor device to mount them on the module board after the step of arranging the first semiconductor devices and the second semiconductor device on the module board after the step of arranging the first and second devices, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module. Therefore, it would have been obvious to incorporate the simultaneous soldering of the first and second devices of Carpenter, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module.

With respect to Claims 50 and 64, one skilled in the art would readily recognize having protruding terminals arranged in rows and columns between each of the DRAM semiconductor chips of the first semiconductor devices and the module board, since the arrangement provides a multiplicity of electrical connection that would increase the signals between the devices and the board. Therefore, it would have been obvious to incorporate terminal arranged in rows and columns between each of the DRAM semiconductor chips of the first semiconductor devices and the module board of Carpenter, since the arrangement provides a multiplicity of electrical connection that would increase the signals between the devices and the board.

With respect to Claims 51 and 65, Carpenter teaches wherein each of the outer leads of the second semiconductor device 60 is exposed to the air between the package body and a portion of the outer leads that connect to the module board (see Figs. 5-7).

With respect to Claims 52 and 66, Carpenter teaches wherein each of the DRAM semiconductor chips 58 of the first semiconductor devices has a main surface and bonding electrodes on the main surface, and wherein the protruded terminals are arranged over the main surface and electrically connected to the bonding electrodes (see col. 4 lines 5-15; Figs. 6).

With respect to Claims 53 and 67, Carpenter teaches wherein the mounting step is performed so that the main surfaces of the DRAM semiconductor chips of the first semiconductor devices face the module board (see Fig. 6).

With respect to Claims 54 and 68, Carpenter teaches wherein in surface of the DRAM semiconductor the mounting step, the back chip of each of the first semiconductor devices 58 are exposed (see Fig. 5).

With respect to Claims 55 and 69, Carpenter teaches sealing a space between each of the first semiconductor devices 58 and the module board 52 with resin 76 (see col. 4 lines 60-67; Fig. 6).

With respect to Claims 56 and 70, Carpenter discloses wherein all protruded terminals of each of the first semiconductor devices 58 are arranged between the corresponding semiconductor chip of the corresponding first semiconductor device and the module board 52 (see Fig. 6).

With respect to Claims 60 and 72, Carpenter disclose in col. 5 lines 3 –10 that the components (i.e. devices 58 and 60) can be arranged differently without requiring modifications in the case 44. Thus, Carpenter in a different arrangement includes a wherein the number of first devices 58 is larger than that of the second device on the module board.

With respect to Claims 62 and 74, Carpenter disclose in the background of the invention that integrated circuits solder attached to connection spots (i.e. terminals) on a printed wiring board (see col. 1 lines 59-67). Thus, the outer leads of the second devices 60 are soldered to the module board.

Conclusion

13. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571)

272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

AC/November 13, 2004

Alonzo Chambliss
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